IN THE CLAIMS:

Please amend Claims 17 and 18 to read as follows. In accordance with the Revised Amendment Format, the status of pending Claims 17 and 18, and the markings in these claims, are presented below.

17. (~~Currently amended) A memory controller~~ comprising:

a converter section adapted to perform serial/parallel conversion of image data ~~of an inputted bit width into image data of ax2n bit width~~ of a bit width inputted into image data of ax2n-bit width;

a first FIFO (first-in-first-out) section adapted to temporarily store the image ~~data of ax2n bit width~~;

a frame memory section adapted to store image data of one frame~~, based on a signal from said first FIFO~~; and

a second FIFO section adapted to temporarily store image data read out from said frame memory section, ~~and~~ wherein

~~a control unit adapted to perform a control process, such that~~ the image data is read out from said first FIFO section, written into said frame memory section, and read out from said frame memory section at a rate that is half of a rate at which the image data is inputted into said first FIFO section, ~~wherein said first FIFO section is of a size suitable for storing image data inputted during a period that equals a sum of a period for reading image data from said frame memory unit a plurality of times and a period necessary for command of said frame memory unit~~ and, within a period for inputting the image data into said first FIFO to FULL capacity, writing the image data into said frame memory section, ~~a plural~~

times of reading the image data from said frame memory section, and executing a command of said frame memory section are conducted.

2 ~~18.~~ (Currently amended) A liquid crystal display comprising:

a liquid crystal panel;

a decoder adapted to convert an inputted image signal into an image signal adaptable to said liquid crystal panel,

wherein said decoder is provided with a memory controller according to ~~Claim 1~~ Claim ~~17~~ 1.

El cncld